

FIG. 1

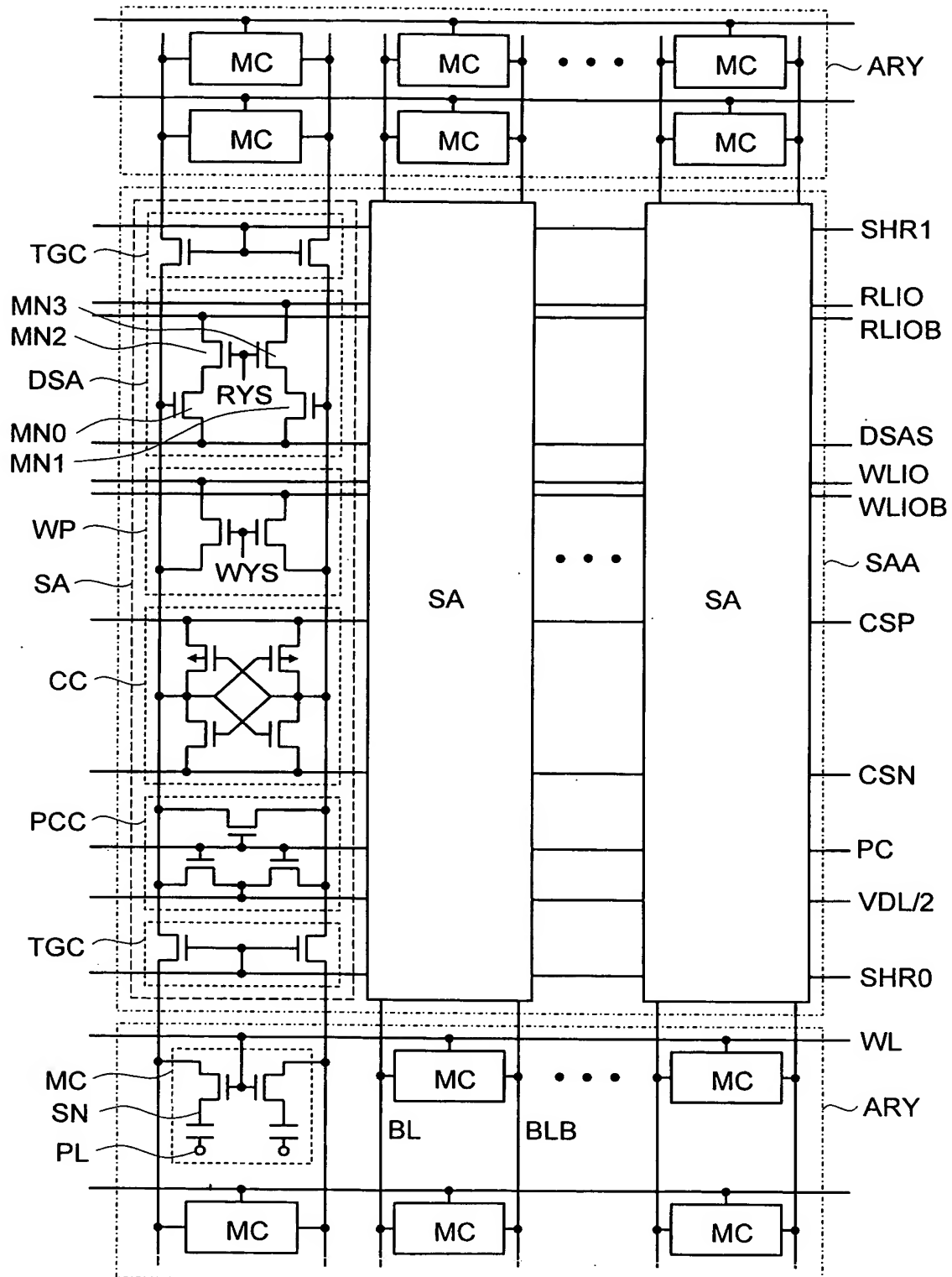


FIG. 2A

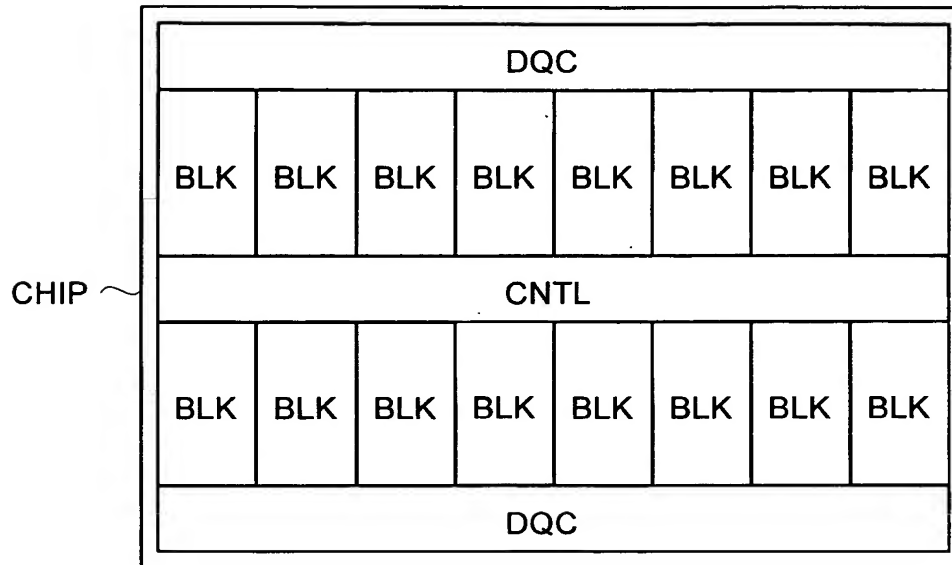


FIG. 2B

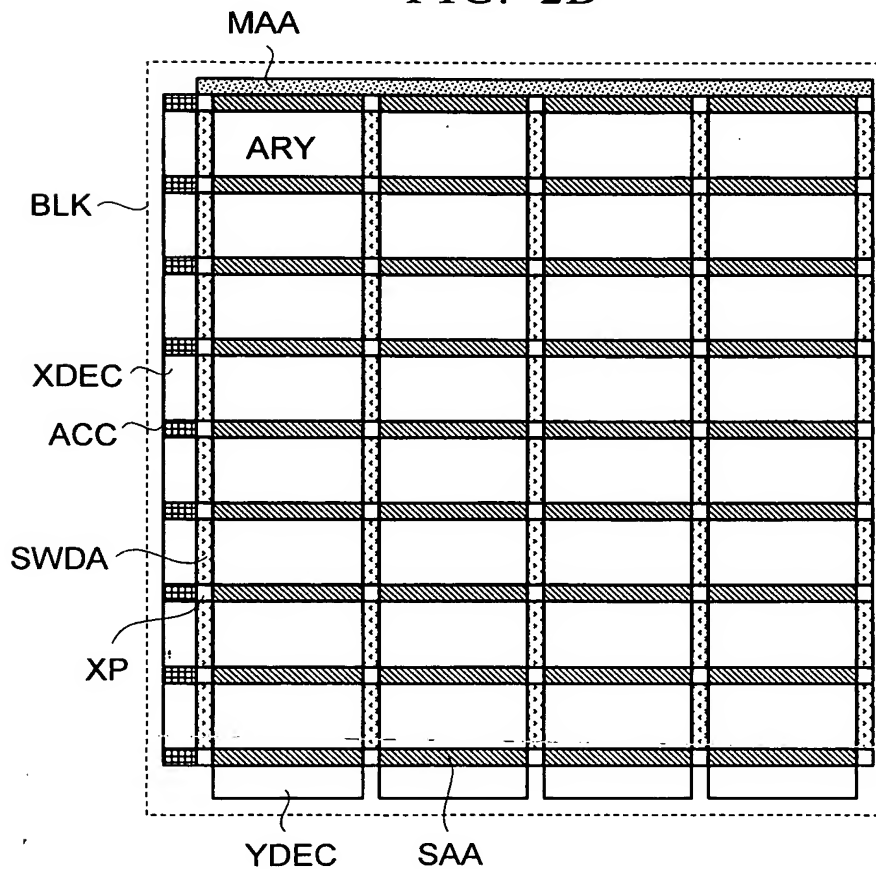


FIG. 3A

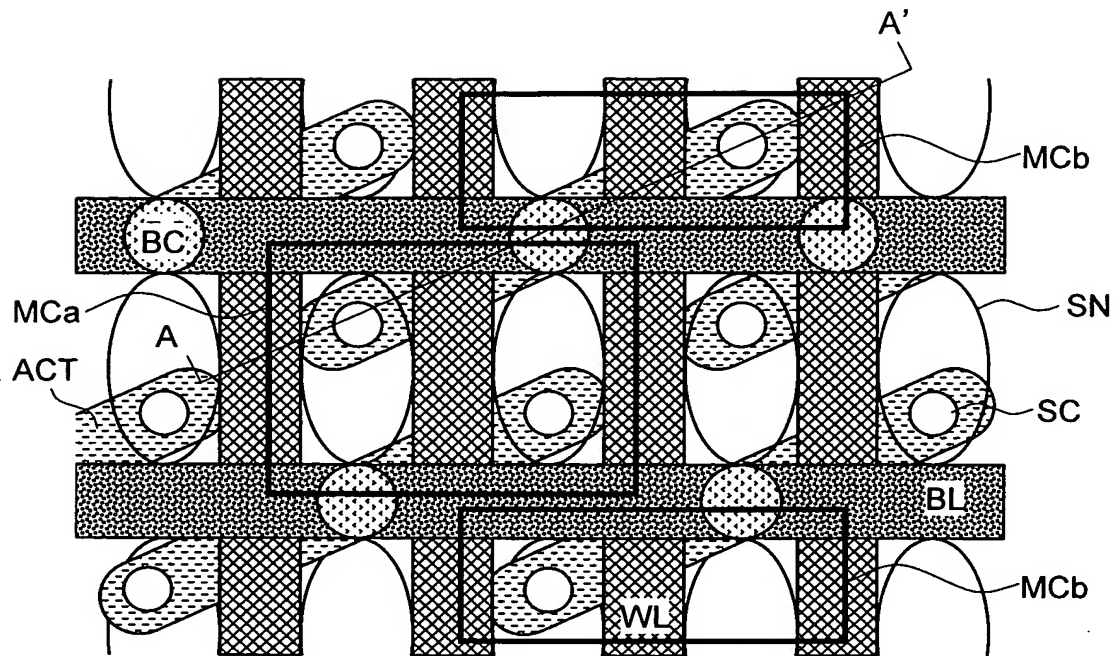
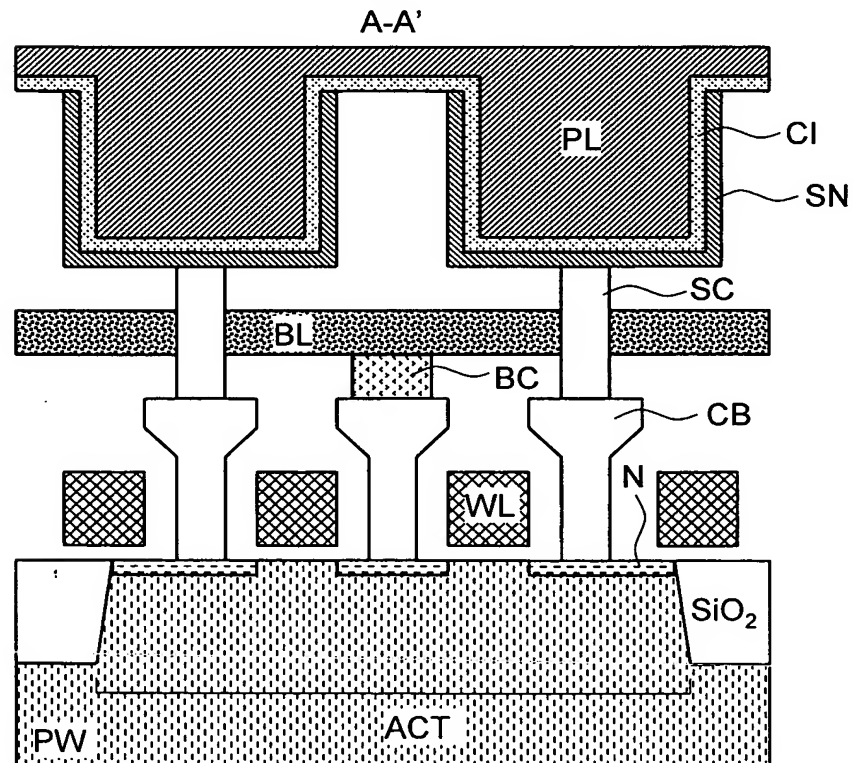


FIG. 3B



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FIG. 4

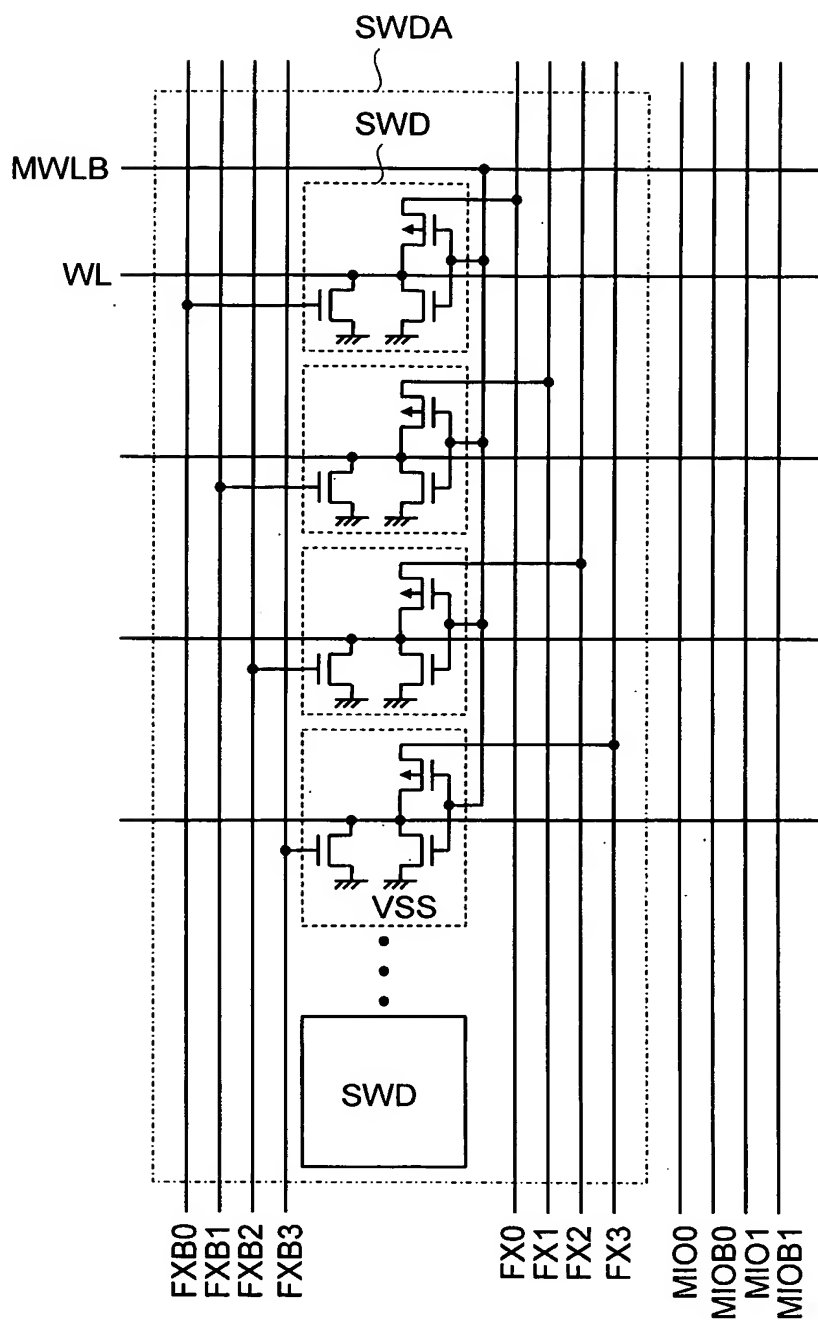


FIG. 5

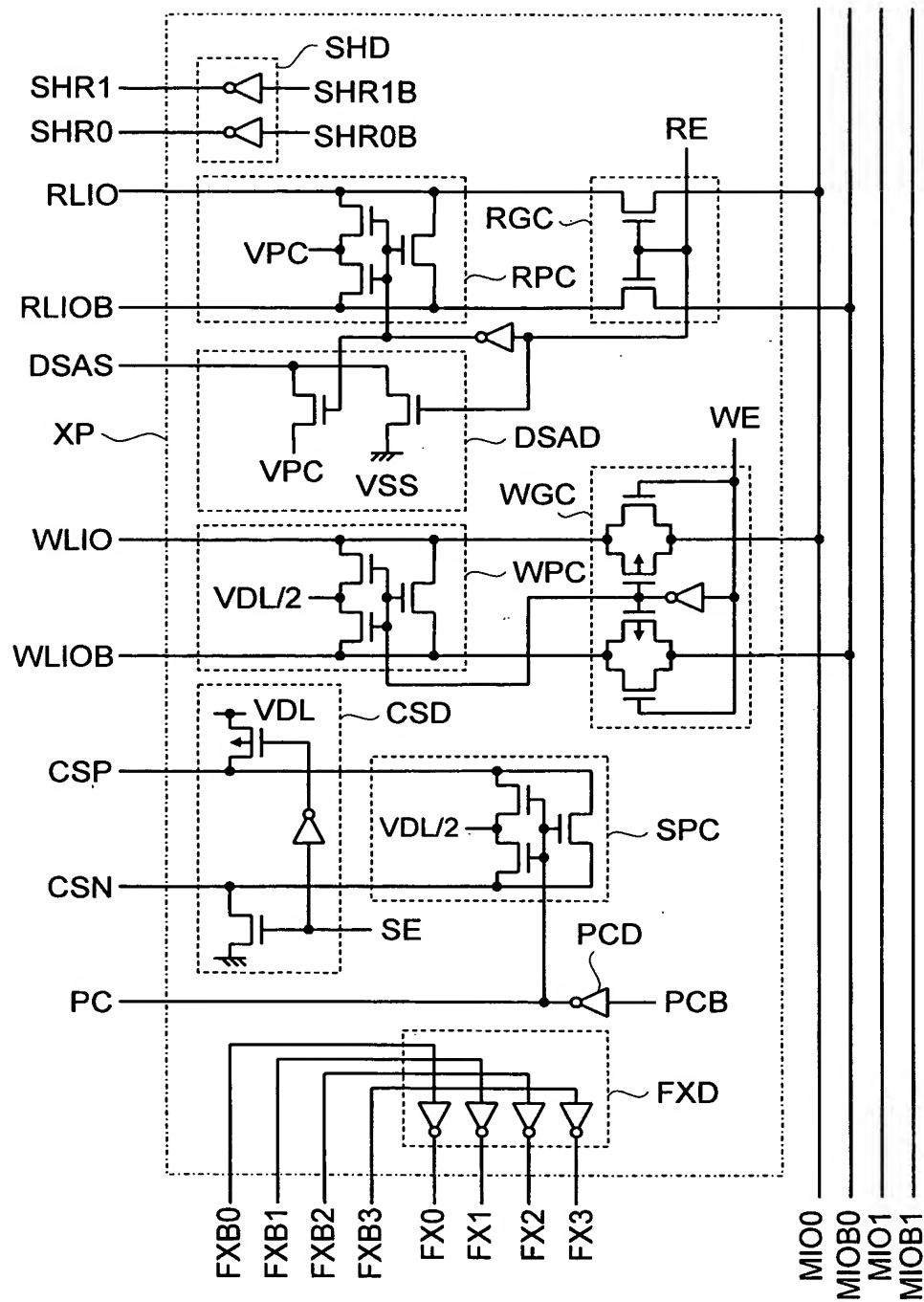
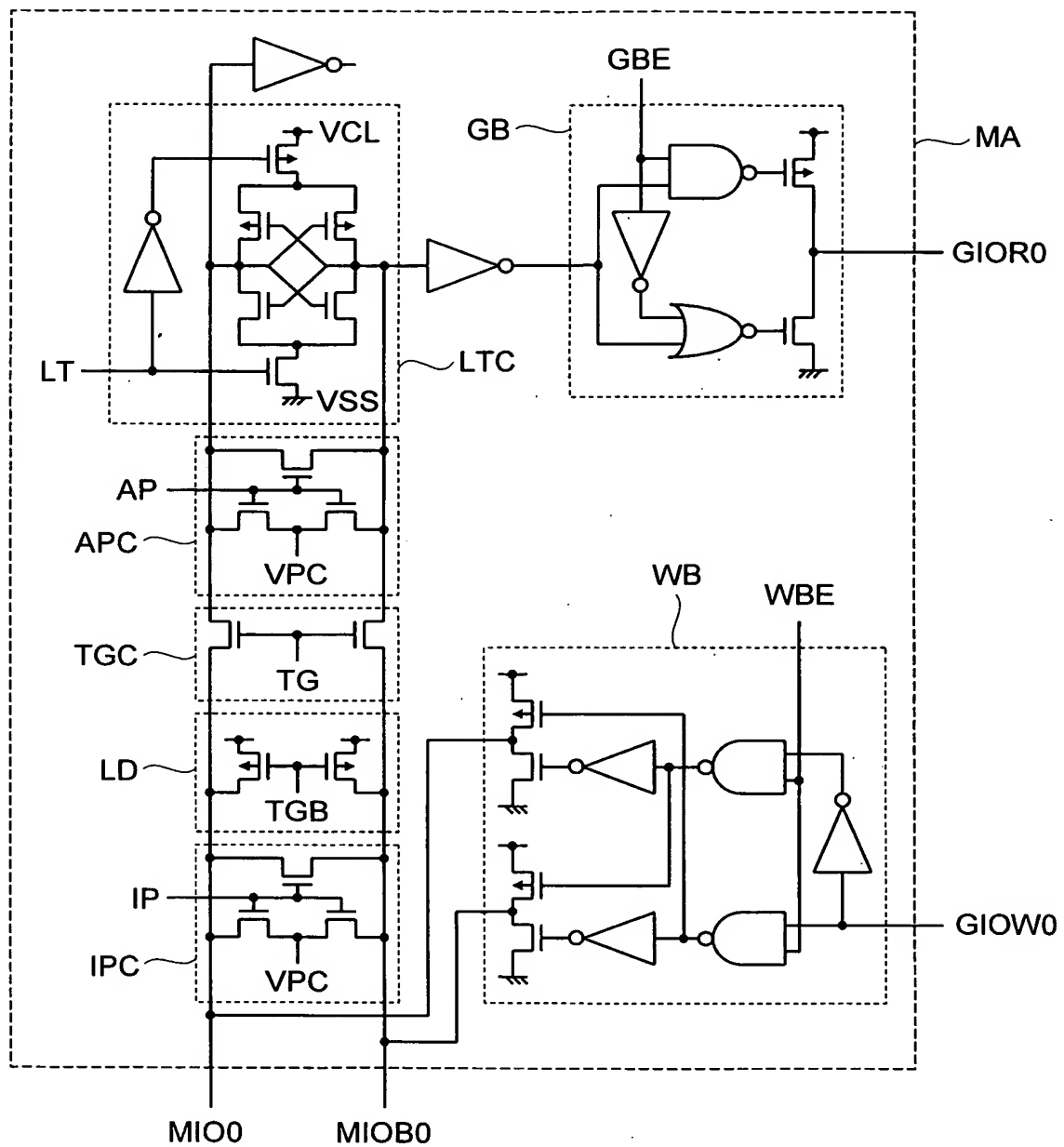


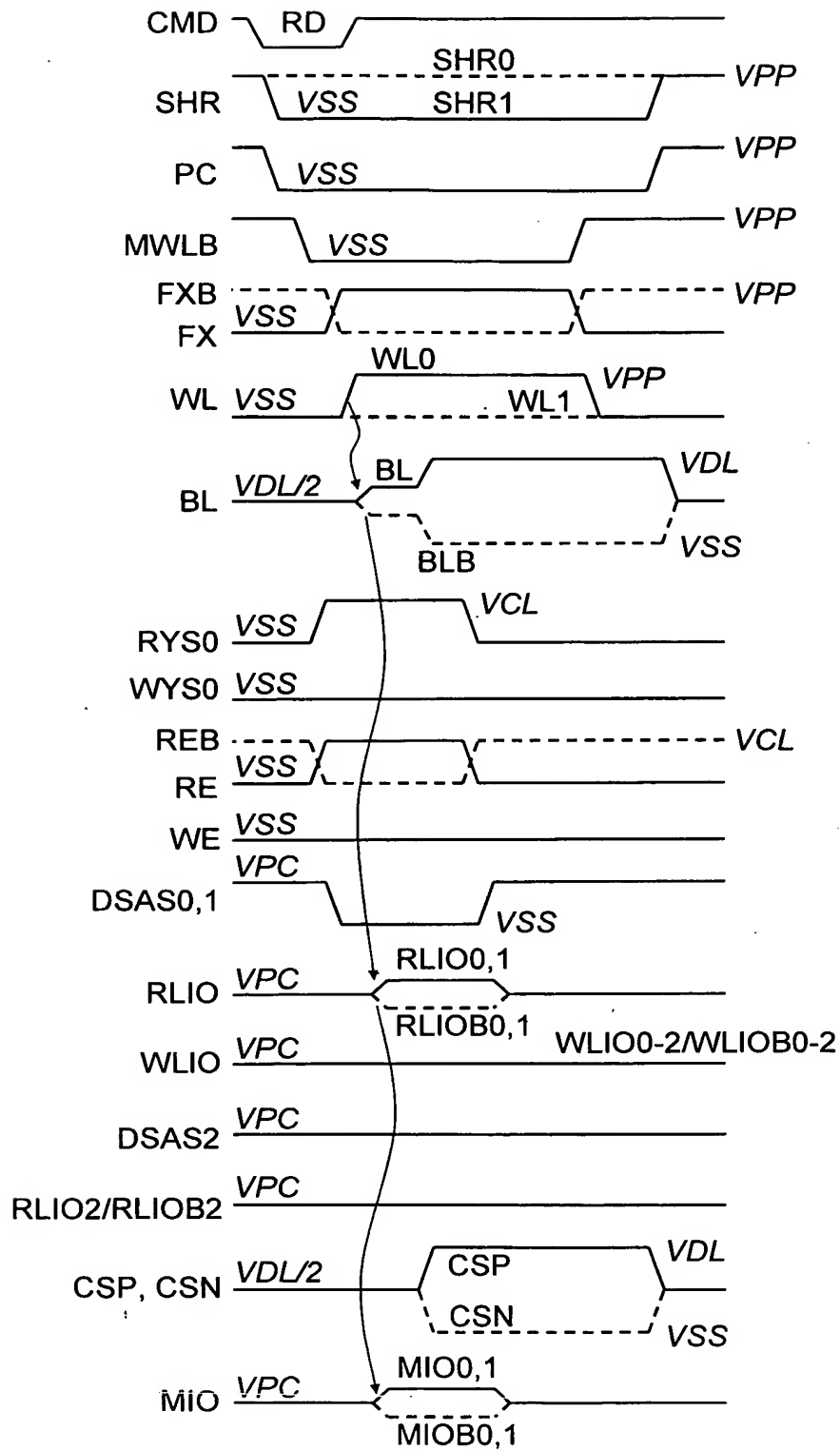
FIG. 6



[illegible]

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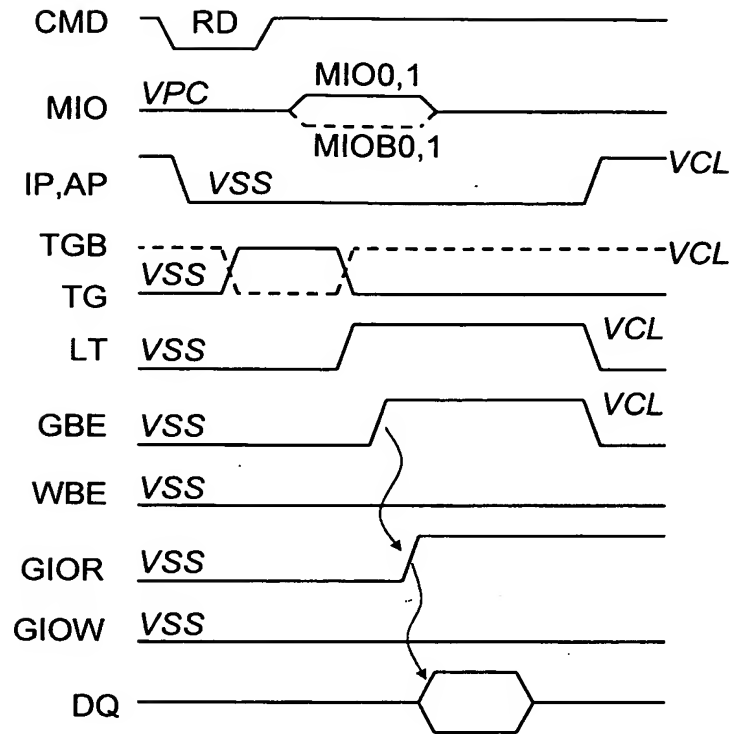
FIG. 8





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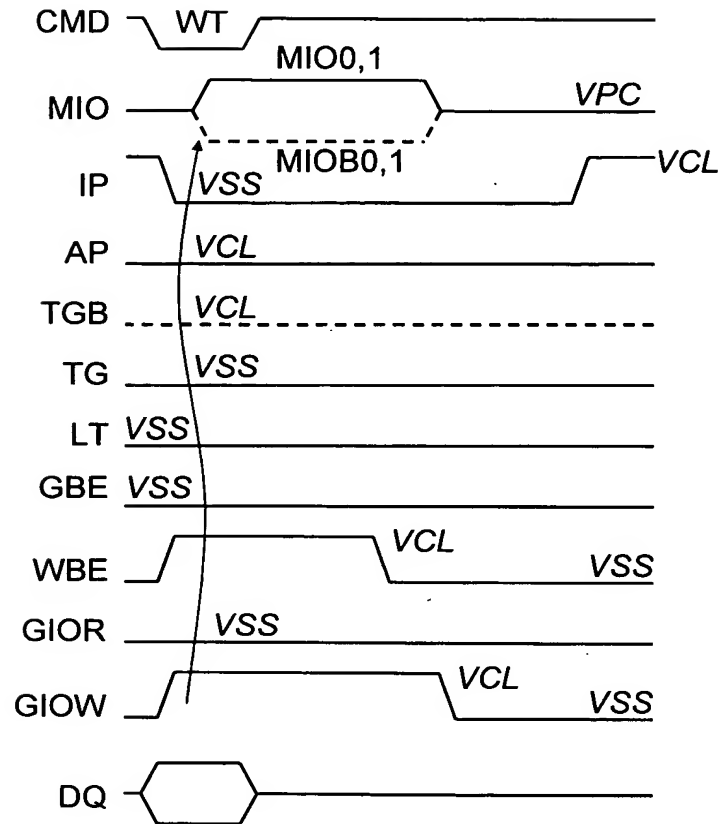
FIG. 9





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FIG. 11



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FIG. 12

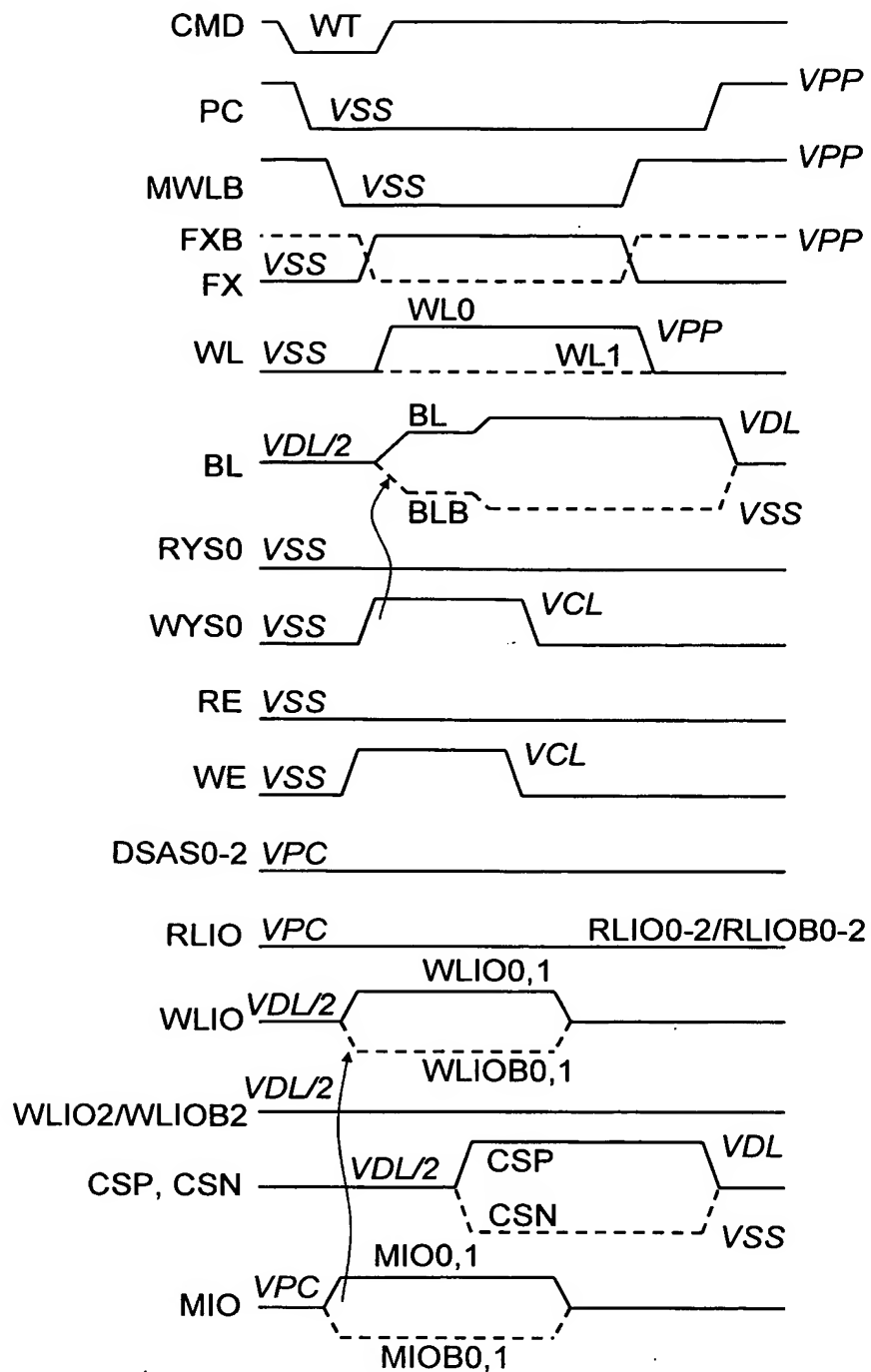
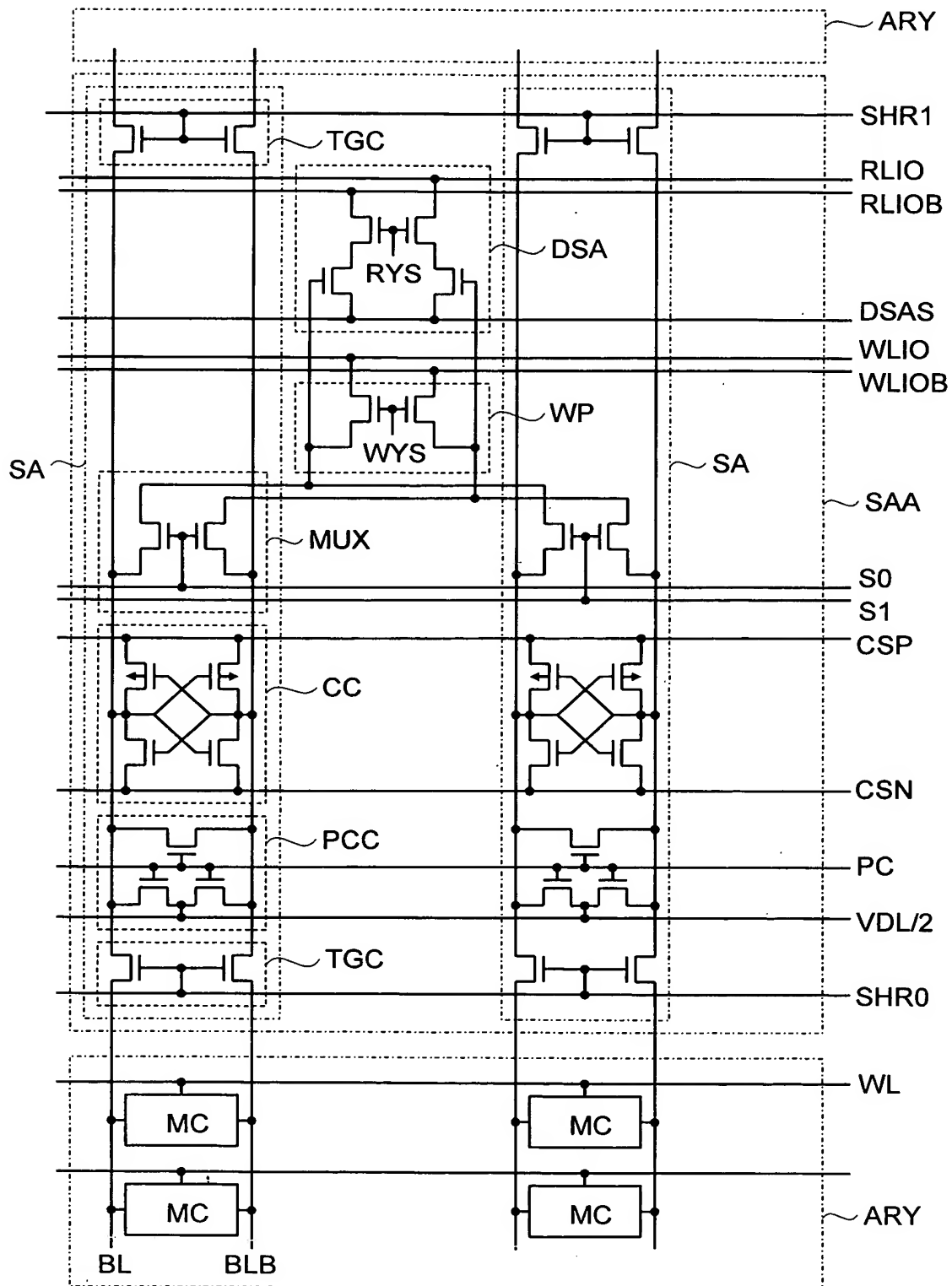


FIG. 13



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FIG. 14

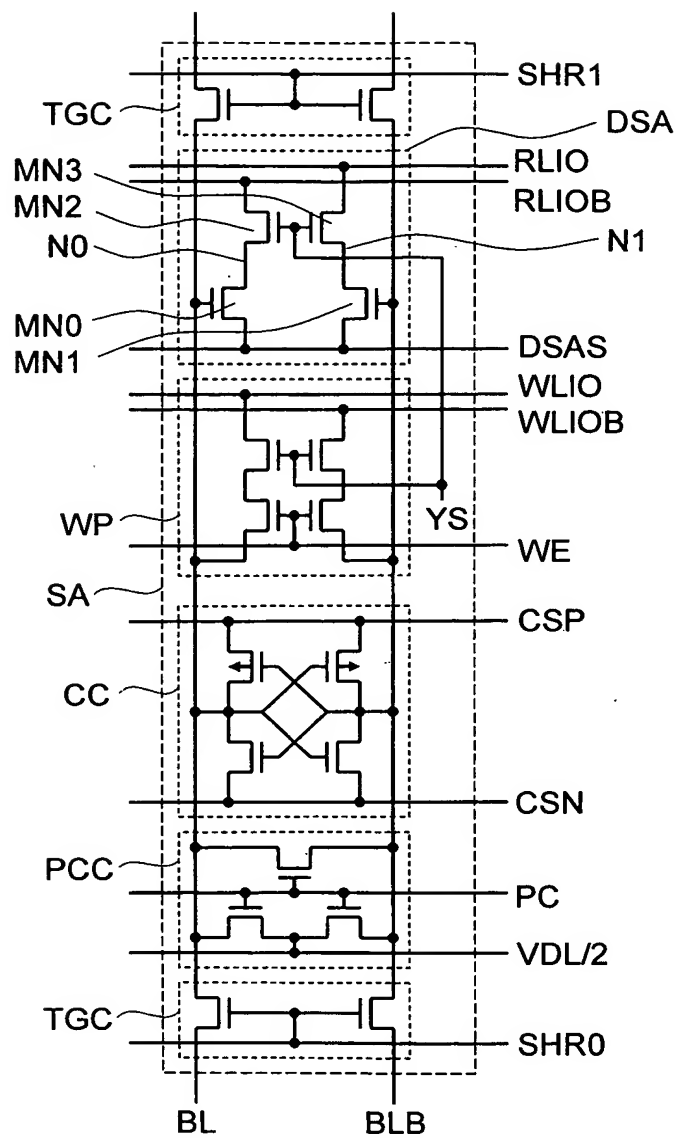
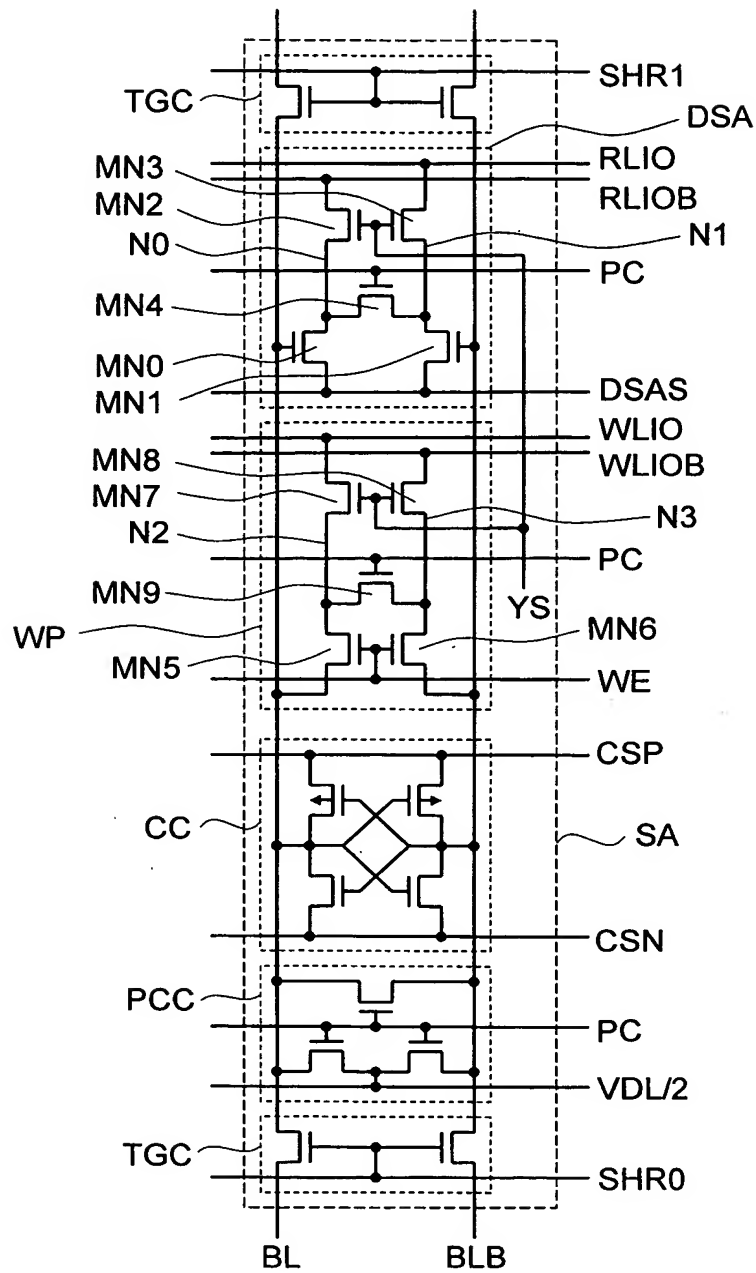


FIG. 15



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FIG. 16

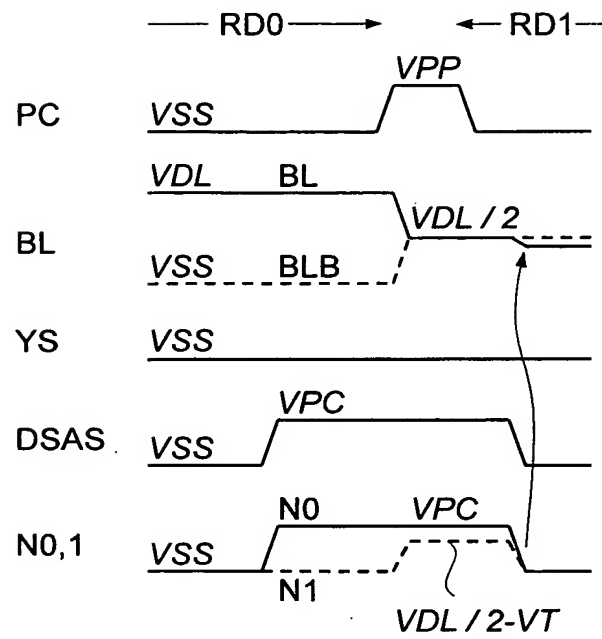
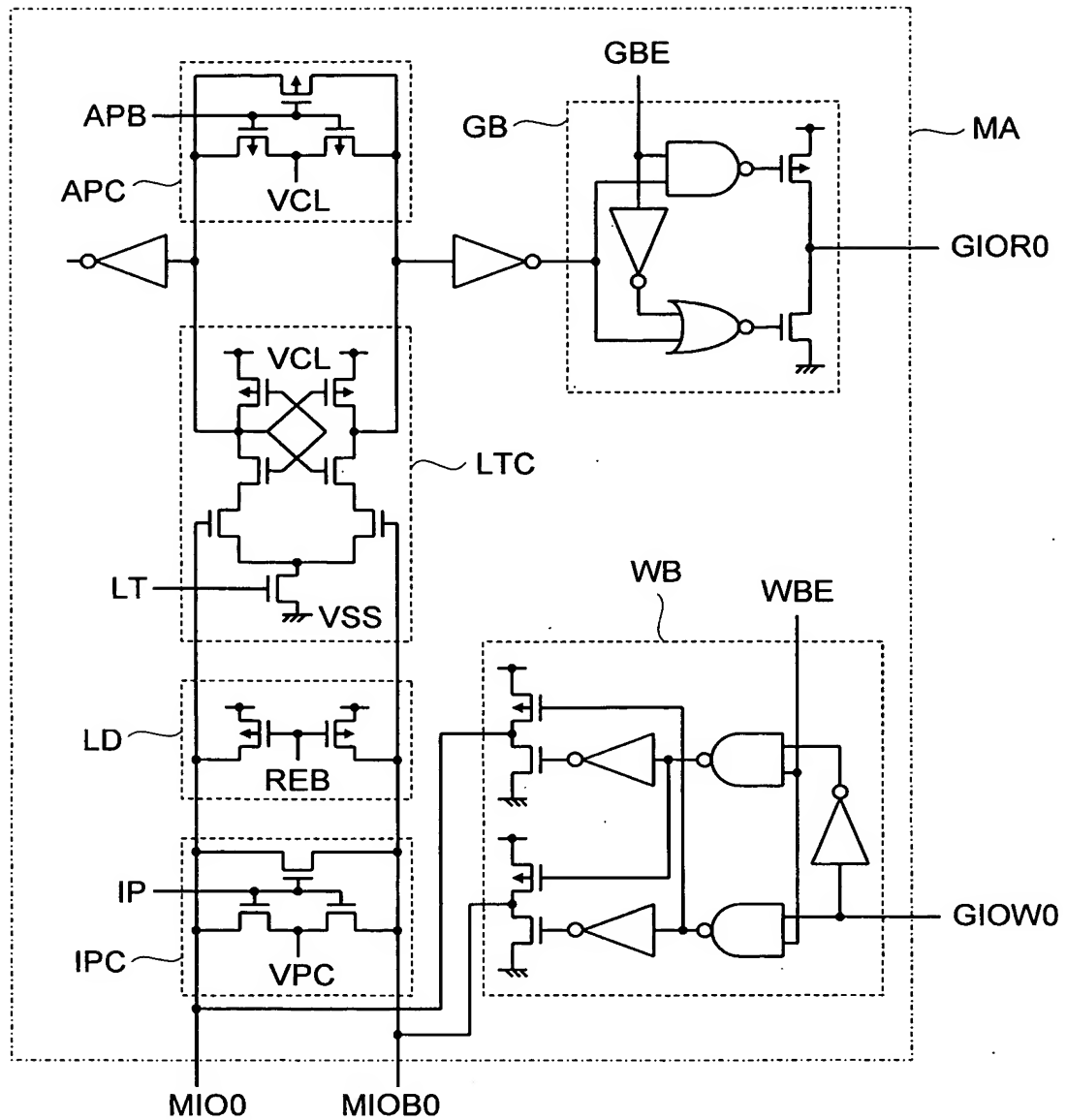


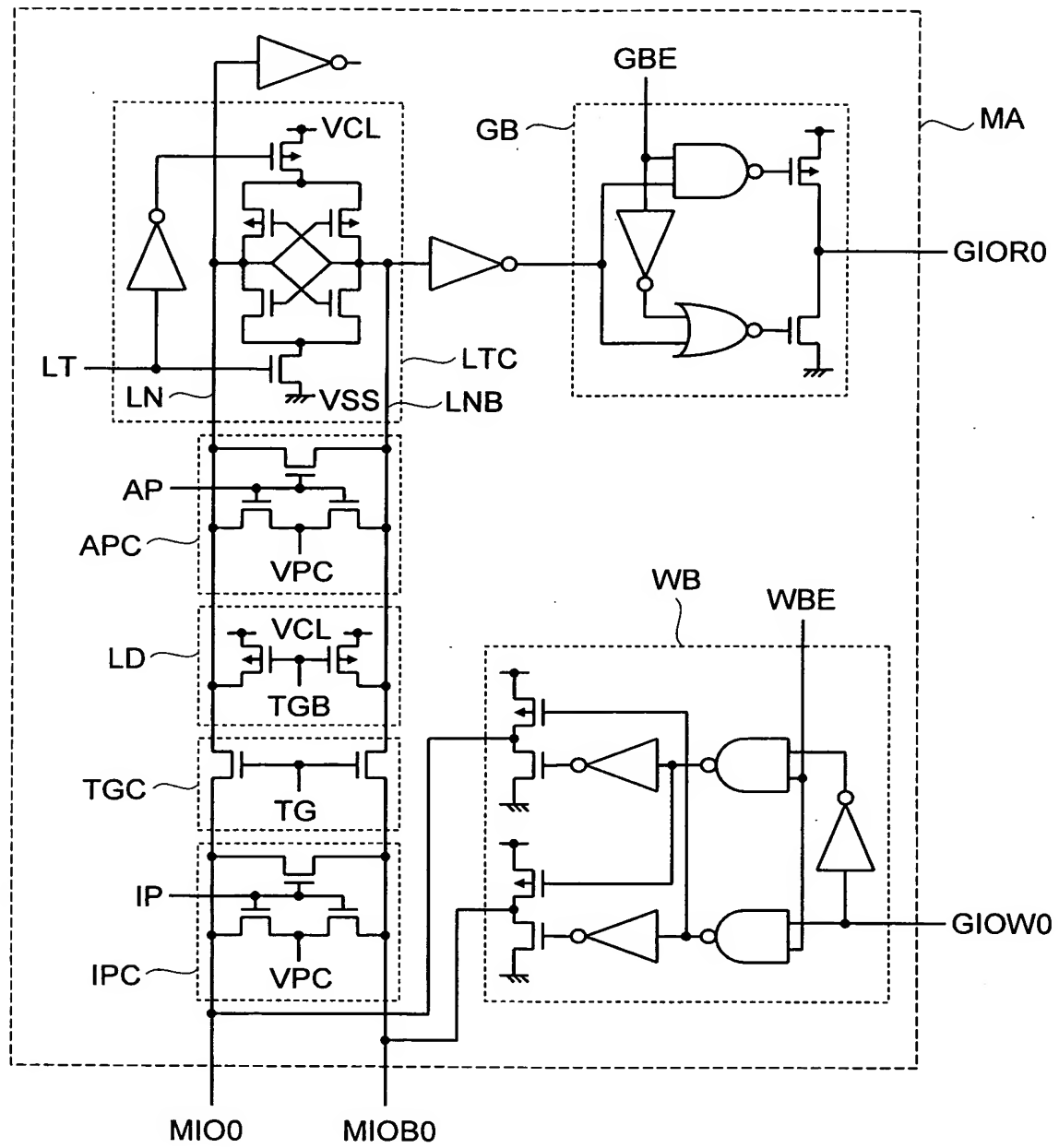


FIG. 17



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FIG. 18



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FIG. 19

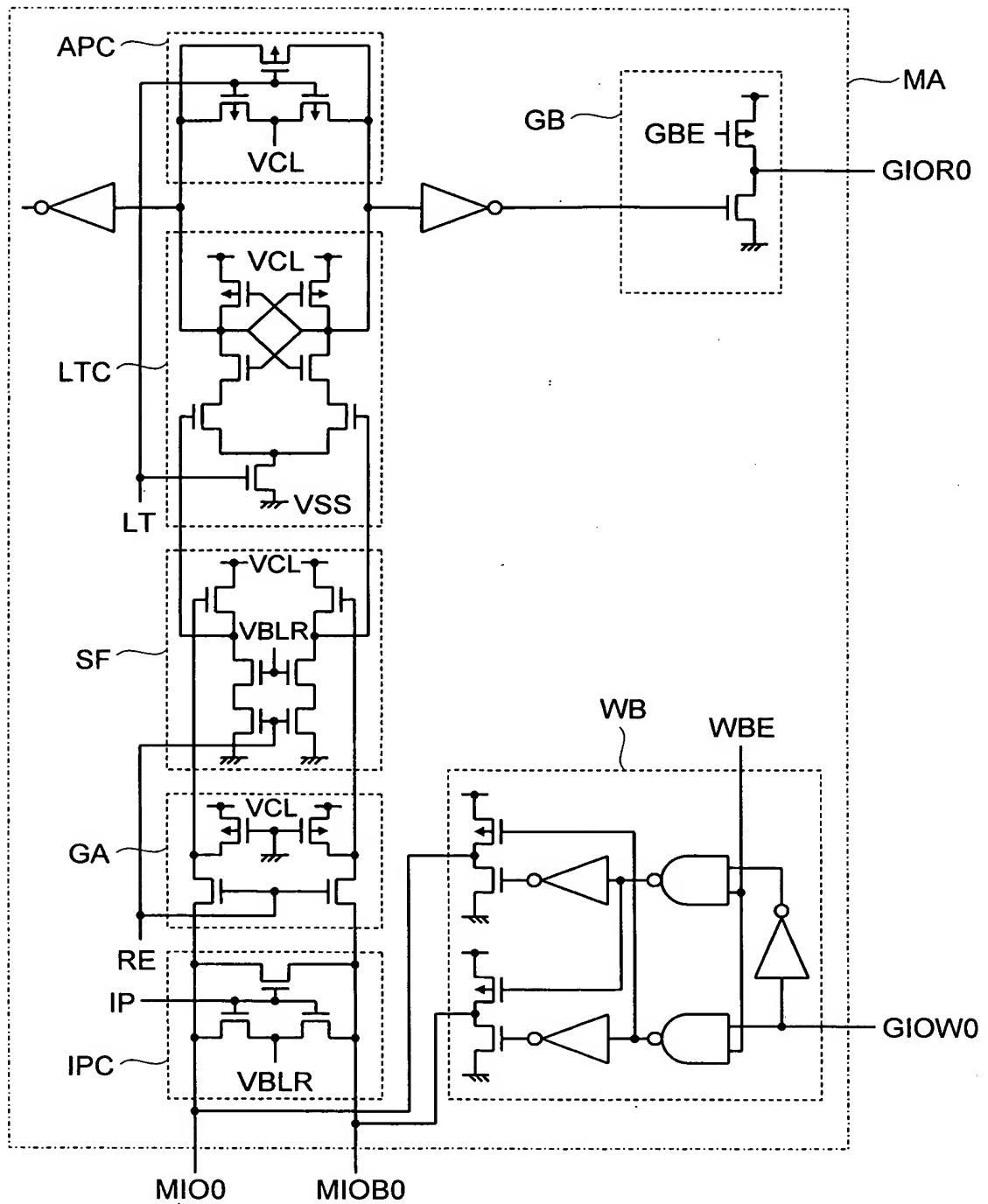
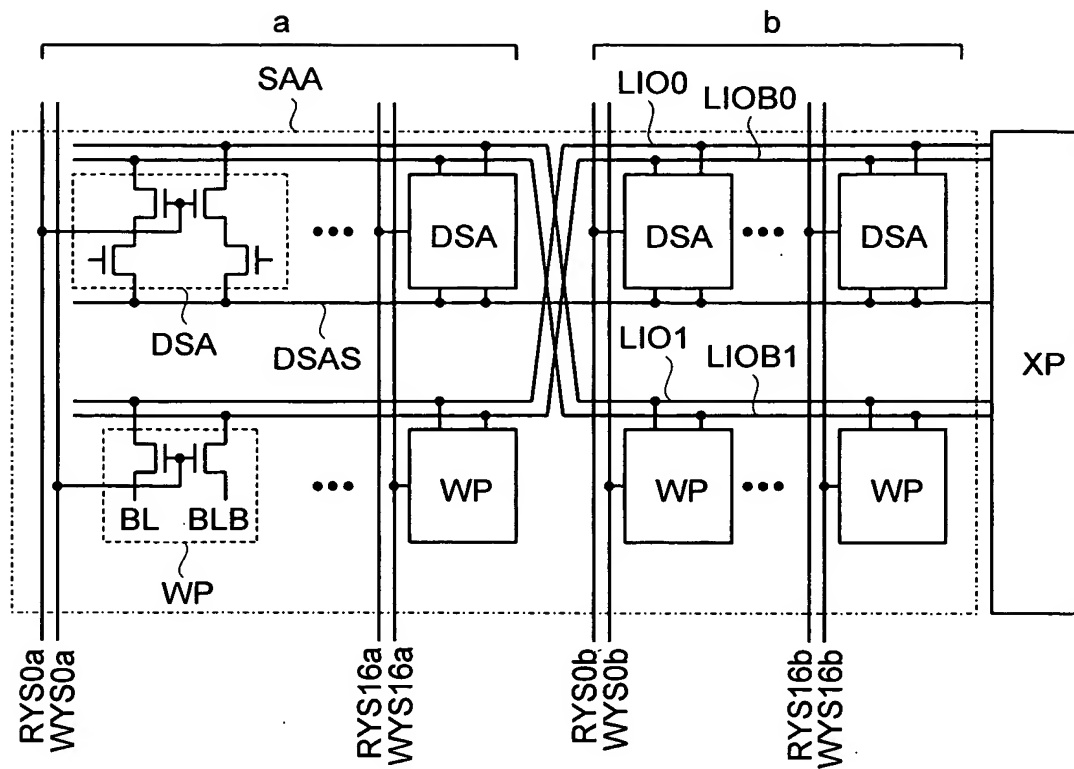


FIG. 20



The diagram illustrates a semiconductor device with a memory array and a peripheral control circuit. The memory array is divided into two main sections: a left section labeled 'ARY' and a right section labeled 'XP'.

**Left Section (ARY):**

- SA (Sense Amplifier):** Located at the top left, connected to the **RLIO** line.
- RLIO (Read Line Input/Output):** A horizontal line running across the top of the array.
- RLIOB (Read Line Input/Output Buffer):** A buffer circuit connected to the **RLIO** line.
- DSA (Data Sense Amplifier):** A circuit block containing the **RYS** (Read Y-Sense) transistor.
- DSAS (Data Sense Amplifier Sense):** A circuit block containing the **PC** (Precharge) transistor.
- PCC (Precharge Control Circuit):** A circuit block containing the **VBLR** (Vertical Bias Line Read) transistor.
- MC (Memory Cell):** A central component connected to the **WL** (Word Line) and **BL** (Bit Line) lines.
- WL (Word Line):** A horizontal line running across the array.
- BL (Bit Line):** A vertical line on the left side of the array.
- BLB (Bit Line Bias):** A vertical line on the right side of the array.

**Right Section (XP):**

- MIOB (Memory Input/Output Buffer):** A buffer circuit at the top right.
- MIO (Memory Input/Output):** A vertical line on the far right.
- ITG (Input/Output Transistor Gate):** A gate connected to the **MIOB** and **MIO** lines.
- RGC (Read Gate Control):** A circuit block containing the **BA** (Bias Amplifier) transistor.
- BA (Bias Amplifier):** A circuit block containing the **REB** (Read Bias) transistor.
- CP (Control Point):** A circuit block containing the **GT** (Gate Transistor) and **GB** (Gate Bias) transistors.
- GT (Gate Transistor):** A transistor connected to the **CP** and **GB** lines.
- GB (Gate Bias):** A transistor connected to the **CP** and **GB** lines.
- RE (Read Enable):** A transistor connected to the **REB** and **REB** lines.
- LD (Load):** A circuit block containing the **LD** (Load) transistor.
- LPC (Load Control Point):** A circuit block containing the **VPC** (Vertical Precharge) transistor.
- VPC (Vertical Precharge):** A transistor connected to the **LPC** and **VPC** lines.

The diagram shows the electrical connections and components of the device, including various transistors, buffers, and control lines.

FIG. 22

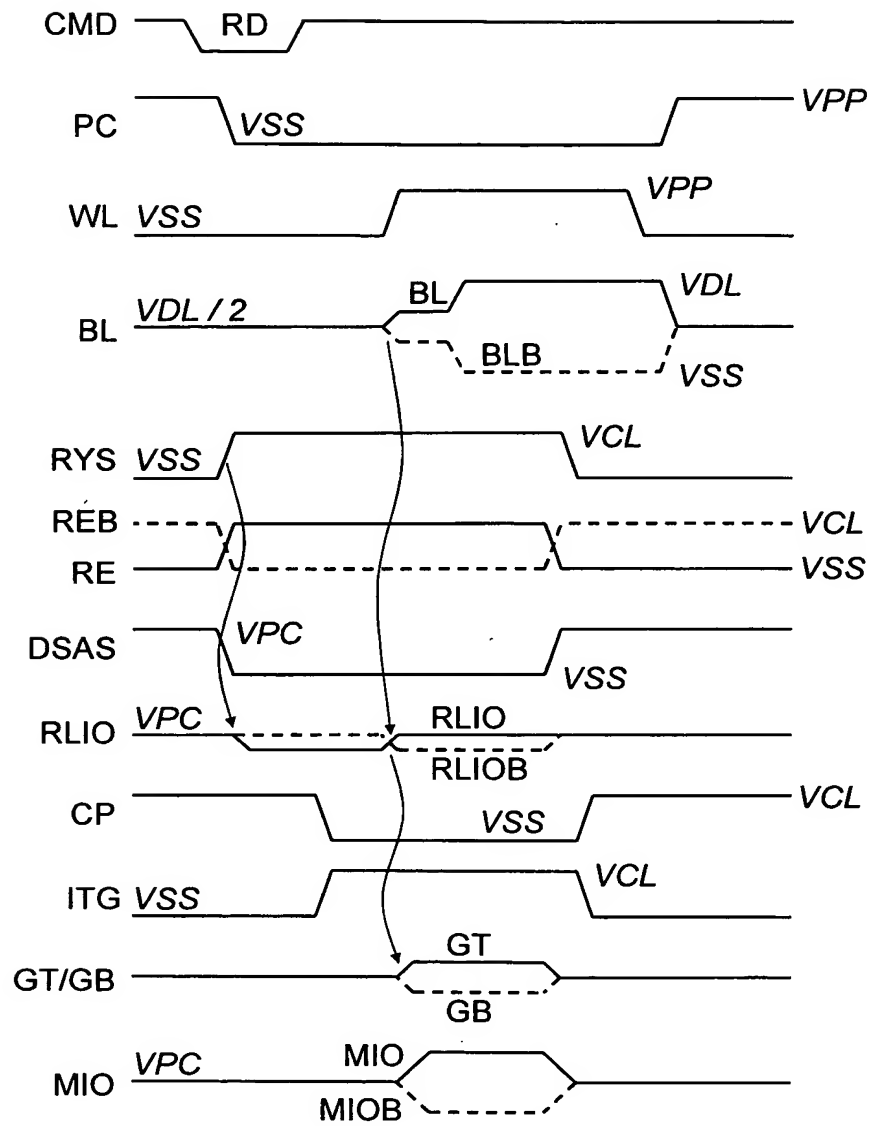


FIG. 23

